DATA SHEET

PCK953

20-125 MHz PECL input / 9 CMOS output
3.3 V PLL clock driver

Product data
Supersedes data of 2003 May 02

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Philips
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20-125 MHz PECL input / 9 CMOS output 3.3 V PLL clock driver

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DESCRIPTION

The PCK953 is a 3.3 V compatible, PLL-based clock driver device targeted for high performance clock tree designs. With output frequencies of up to 125 MHz, and output skews of 100 ps, the PCK953 is ideal for the most demanding clock tree designs. The devices employ a fully differential PLL design to minimize cycle-to-cycle and phase jitter.

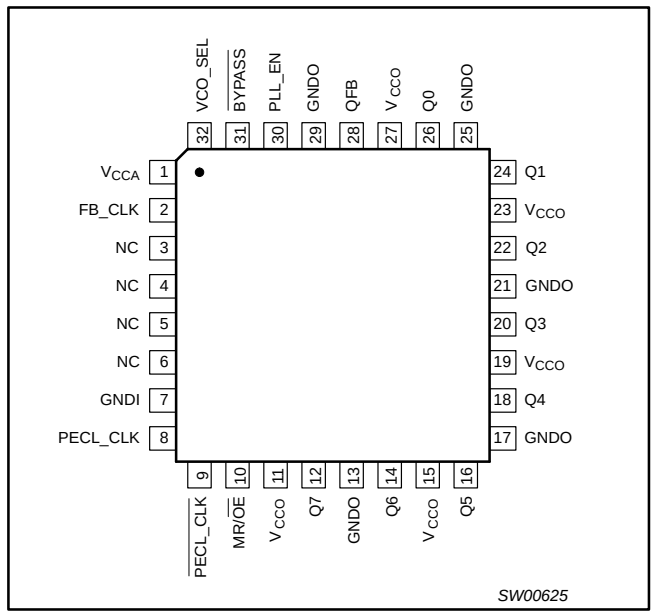
The PCK953 has a differential LVPECL reference input, along with an external feedback input. These features make the PCK953 ideal for use as a zero delay, low skew fanout buffer. The device performance has been tuned and optimized for zero delay performance. The MR/$\overline{OE}$ input pin will reset the internal counters and 3-State the output buffers when driven HIGH.

The PCK953 is fully 3.3 V compatible and requires no external loop filter components. All control inputs accept LVCMOS or LVTTL compatible levels, while the outputs provide LVCMOS levels with the ability to drive terminated 50 Ω transmission lines. For series terminated 50 Ω lines, each of the PCK953 outputs can drive two traces, giving the device an effective fanout of 1:18. The device is packaged in a 7 × 7 mm 32-lead LQFP package to provide the optimum combination of board density and performance.

FEATURES

- Fully integrated PLL
- Output frequency up to 125 MHz in PLL mode
- Outputs disable in high impedance
- LQFP32 packaging
- 55 ps cycle-to-cycle jitter typical
- 9 mA quiescent current, I_{CCA}, typical
- 60 ps static phase offset typical
- Less than 10 μA quiescent current, I_{CCO}, typical

PIN CONFIGURATION



PIN DESCRIPTION

PIN NUMBER	SYMBOL	FUNCTION
1	V_{CCA}	Analog supply voltage. See Application Information section for design and layout considerations.
2	FB_CLK	Feedback clock input (CMOS) to comparator / phase detector
3-6	NC	Not connected
7	GNDI	Ground pin associated with input circuitry
8	PECL_CLK	LVPECL reference clock input, true
9	$\overline{PECL\_CLK}$	LVPECL reference clock input, complementary
10	MR/$\overline{OE}$	Master Reset / Output Enable input. See Function Table
11, 1519, 23, 27	V_{CCO}	Supply voltage pins associated with output driver circuitry
12, 14, 16, 18, 20, 22, 24, 26	Q7-Q0	Buffered clock outputs (CMOS)
13, 17, 21, 25, 29	GNDO	Ground pins associated with output driver circuitry
28	QFB	Buffered clock output intended to be fed to feedback pin FB_CLK
30	PLL_EN	PLL Enable input pin. See Function Table
31	$\overline{BYPASS}$	Bypass input pin. See Function Table
32	VCO_SEL	VCO Select input pin. See Function Table

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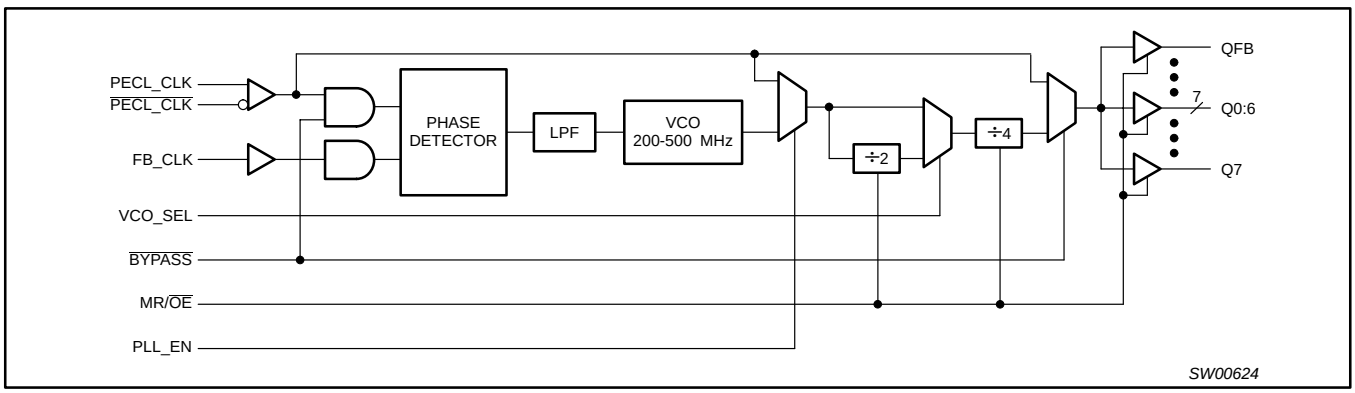
ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	ORDER CODE	DRAWING NUMBER
LQFP32 plastic low profile quad flat package; 32 leads	0 to +70 °C	PCK953BD	SOT358-1

LOGIC DIAGRAM



FUNCTION TABLE

$\overline{\text{BYPASS}}$	Function
1	PLL Enabled
0	PLL Bypass
MR/$\overline{\text{OE}}$	**Function**
1	Outputs Disabled
0	Outputs Enabled
VCO_SEL	**Function**
1	÷2
0	÷1
PLL_EN	**Function**
1	Select VCO
0	Select PECL_CLK

ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	PARAMETER	MIN	MAX	UNIT
V_{CC}	Supply voltage	-0.3	4.6	V
V_I	Input voltage	-0.3	V_{DD}+0.3	V
I_{IN}	Input current	—	±20	mA
T_{stg}	Storage temperature range	-40	+125	°C

NOTE:

1. Absolute maximum continuous ratings are those values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation under absolute-maximum-rated conditions is not implied.

DC CHARACTERISTICS

T_{amb} = 0 to 70°C; V_{CC} = 3.3 V ±5%

SYMBOL	PARAMETER	CONDITION	MIN	TYP	MAX	UNIT
V_{IH}	HIGH-level input voltage LVCMOS inputs		2.0	—	3.6	V
V_{IL}	LOW-level input voltage LVCMOS inputs		—	—	0.8	V
V_{p-p}	Peak-to-peak input voltage PECL_CLK		300	—	1000	mV
V_{CMR}	Common mode range PECL_CLK	Note 1	V_{CC}-1.5	—	V_{CC}-0.6	mV
V_{OH}	HIGH-level output voltage	I_{OH} = -20 mA;[2]	2.4	—	—	V
V_{OL}	LOW-level output voltage	I_{OL} = 20 mA;[2]	—	—	0.5	V
I_{IN}	Input current		—	—	±75	µA
C_{IN}	Input capacitance		—	—	4	pF
C_{PD}	Power dissipation capacitance	per output	—	25	—	pF
I_{CC}	Maximum quiescent supply current	All V_{CC} pins	—	9	20	mA
I_{CCPLL}	Maximum PLL supply current	V_{CCA} pin only	—	9	20	mA

NOTES:
1. V_{CMR} is the difference from the most positive side of the differential input signal. Normal operation is obtained when the HIGH input is within the V_{CMR} range and the input swing lies within the V_{PP} specification.
2. The PCK953 outputs can drive series or parallel terminated 50 Ω (or 50 Ω to V_{CC}/2) transmission lines on the incident edge (see 'Applications information' section).

PLL INPUT REFERENCE CHARACTERISTICS

T_{amb} = 0 to 70°C

SYMBOL	PARAMETER	CONDITION	MIN	MAX	UNIT
f_{ref}	Reference input frequency		20	125	MHz
f_{refDC}	Reference input duty cycle		25	75	%

NOTE:
1. Maximum and minimum input reference is limited by the VCO lock range and the feedback divider.

AC CHARACTERISTICS

T_{amb} = 0 to 70°C; V_{CC} = 3.3 V ±5%

SYMBOL	PARAMETER		CONDITION	MIN	TYP	MAX	UNIT
t_r, t_f	Output rise/fall time		0.8 V to 2.0 V	0.30	0.55	0.8	ns
t_{pw}	Output duty cycle			45	50	55	%
$t_{sk(O)}$	Output-to-output skews (relative to QFB)			—	—	100	ps
f_{VCO}	PLL VCO lock range			120	—	500	MHz
f_{MAX}	Maximum output frequency	PLL mode	VCO_SEL = 1	20	—	100	MHz
			VCO_SEL = 0	35		125	MHz
		Bypass mode				225	MHz
t_{pd}(lock)	Input to EXT_FB delay (with PLL locked)		f_{ref} = 50 MHz	-75	—	125	ps
t_{pd}(by-pass)	Input to Q delay		PLL bypassed	3	5.2	7	ns
t_{PLZ-HZ}	Output disable time			—	—	7	ns
t_{PZL}	Output enable time			—	—	6	ns
t_{jitter}	Cycle-to-cycle jitter (peak-to-peak)			—	55	100	ps
t_{lock}	Maximum PLL lock time			—	0.01	10	ms

NOTE:
1. X will be targeted for 0 ns, but may vary from target by ±150 ps based on characterization of silicon.

APPLICATION INFORMATION

Power supply filtering

The PCK953 is a mixed analog/digital product and as such it exhibits some sensitivities that would not necessarily be seen on a fully digital product. Analog circuitry is naturally susceptible to random noise, especially if this noise is seen on the power supply pins. The PCK953 provides separate power supplies for the output buffers (V_{CCO}) and the phase-locked loop (V_{CCA}) of the device. The purpose of this design technique is to try to isolate the HIGH switching noise digital outputs from the relatively sensitive internal analog phase-locked loop. In a controlled environment such as an evaluation board, this level of isolation is sufficient. However, in a digital system environment where it is more difficult to minimize noise on the power supplies, a second level of isolation may be required. The simplest form of isolation is a power supply filter on the V_{CCA} pin for the PCK953.

Figure 1 illustrates a typical power supply filter scheme. The PCK953 is most susceptible to noise with spectral content in the 1 kHz to 1 MHz range. Therefore, the filter should be designed to target this range. The key parameter that needs to be met in the final filter design is the DC voltage drop that will be seen between the V_{CC} supply and the V_{CCA} pin of the PCK953. From the datasheet, the I_{VCCA} current (the current sourced though the V_{CCA} pin) is typically 15 mA (20 mA maximum), assuming that a minimum of 3.0 V must be maintained on the V_{CCA} pin, very little DC voltage drop can be tolerated when a 3.3 V V_{CC} supply is used. The resistor shown in Figure 1 must have a resistance of 10-15 Ω to meet the voltage drop criteria. The RC filter pictured will provide a broadband filter with approximately 100:1 attenuation for noise whose spectral content is above 20 kHz. As the noise frequency crosses the series resonant point of an individual capacitor, its overall impedance begins to look inductive, and thus increases with increasing frequency. The parallel capacitor combination shown ensures that a low impedance path to ground exists for frequencies well above the bandwidth of the PLL. It is recommended that the user start with an 8-10 Ω resistor to avoid potential V_{CC} drop problems, and only move to the higher value resistors when a higher level of attenuation is shown to be needed.

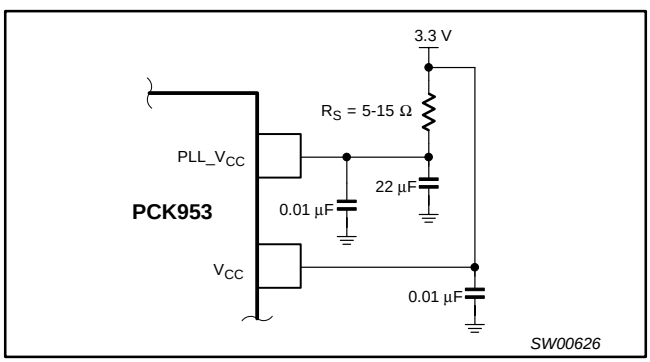


Figure 1. Power supply filter

Although the PCK953 has several design features to minimize the susceptibility to power supply noise (isolated power and grounds and fully differential PLL) there still may be applications in which overall performance is being degraded due to system power supply noise. The power supply filter schemes discussed in this section should be adequate to eliminate power supply noise related problems in most designs.

Driving transmission lines

The PCK953 clock driver was designed to drive high speed signals in a terminated transmission line environment. To provide the optimum flexibility to the user, the output drivers were designed to exhibit the lowest impedance possible. With an output impedance of less than 20 Ω, the drivers can drive either parallel or series terminated transmission lines.

In most high performance clock networks, point-to-point distribution of signals is the method of choice. In a point-to-point scheme either series terminated or parallel terminated transmission lines can be used. The parallel technique terminates the signal at the end of the line with a 50 Ω resistance to V_{CC}/2. This technique draws a fairly high level of DC current, and thus only a single terminated line can be driven by each output of the PCK953 clock driver. For the series terminated case, however, there is no DC current draw, thus the outputs can drive multiple series terminated lines. Figure 2 illustrates an output driving a single series terminated line versus two series terminated lines in parallel. When taken to its extreme, the fanout of the PCK953 clock driver is effectively doubled due to its capability to drive multiple lines.

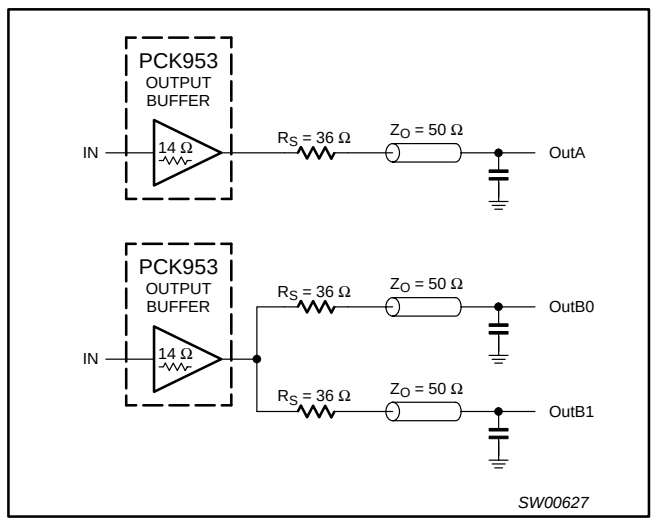


Figure 2. Single versus dual transmission lines

The waveform plots of Figure 3 show the simulation results of an output driving a single line versus two lines. In both cases, the drive capability of the PCK953 output buffers is more than sufficient to drive 50 Ω transmission lines on the incident edge. Note from the delay measurements in the simulations, a delta of only 43 ps exists between the two differently loaded outputs. This suggests that the dual line driving need not be used exclusively to maintain the tight output-to-output skew of the PCK953. The output waveform in Figure 3 shows a step in the waveform; this step is caused by the impedance mismatch seen looking into the driver. The parallel combination of the 43 Ω series resistor plus the output impedance does not match the parallel combination of the line impedances. The voltage wave launched down the two lines will equal:

$VL = VS (Z_O / (R_S + R_O + Z_O))$

$Z_O = 50\ \Omega \parallel 50\ \Omega$

$R_S = 36\ \Omega \parallel 36\ \Omega$

$R_O = 14\ \Omega$

$VL = 3.0 (25 / (18 + 14 + 25) = 3.0 (25 / 57) = 1.31$ V

At the load end, the voltage will double due to the near unity reflection coefficient, to 2.62 V. It will then increment towards the quiescent 3.0 V in steps separated by one round-trip delay (in this case 4.0 ns).

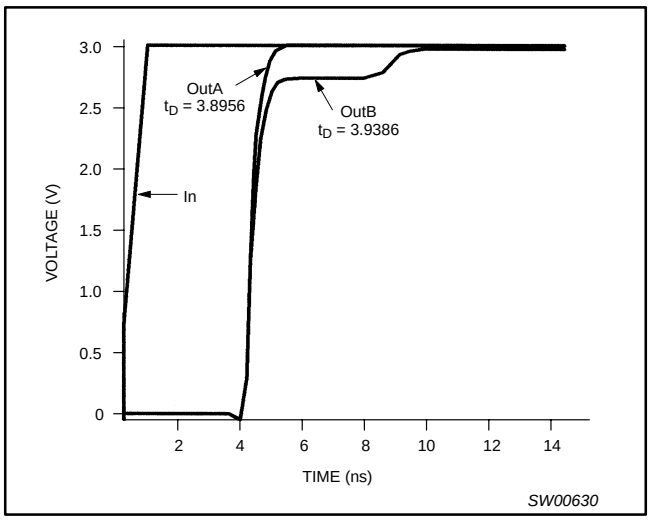


Figure 3. Single versus dual waveforms

Since this step is well above the threshold region, it will not cause any false clock triggering, however designers may be uncomfortable with unwanted reflections on the line. To better match the impedances when driving multiple lines, the situation in Figure 4 should be used. In this case, the series terminating resistors are reduced such that when the parallel combination is added to the output buffer impedance, the line impedance is perfectly matched.

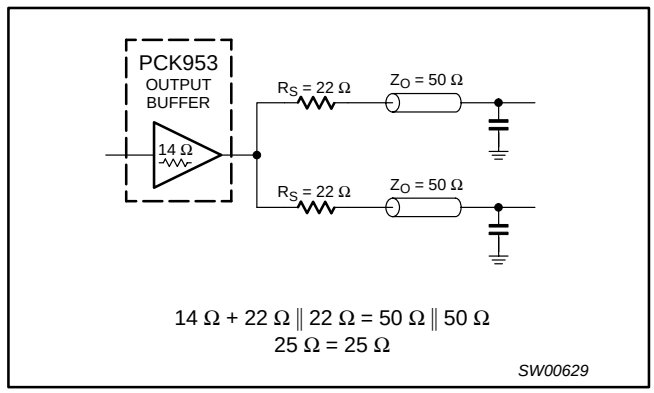
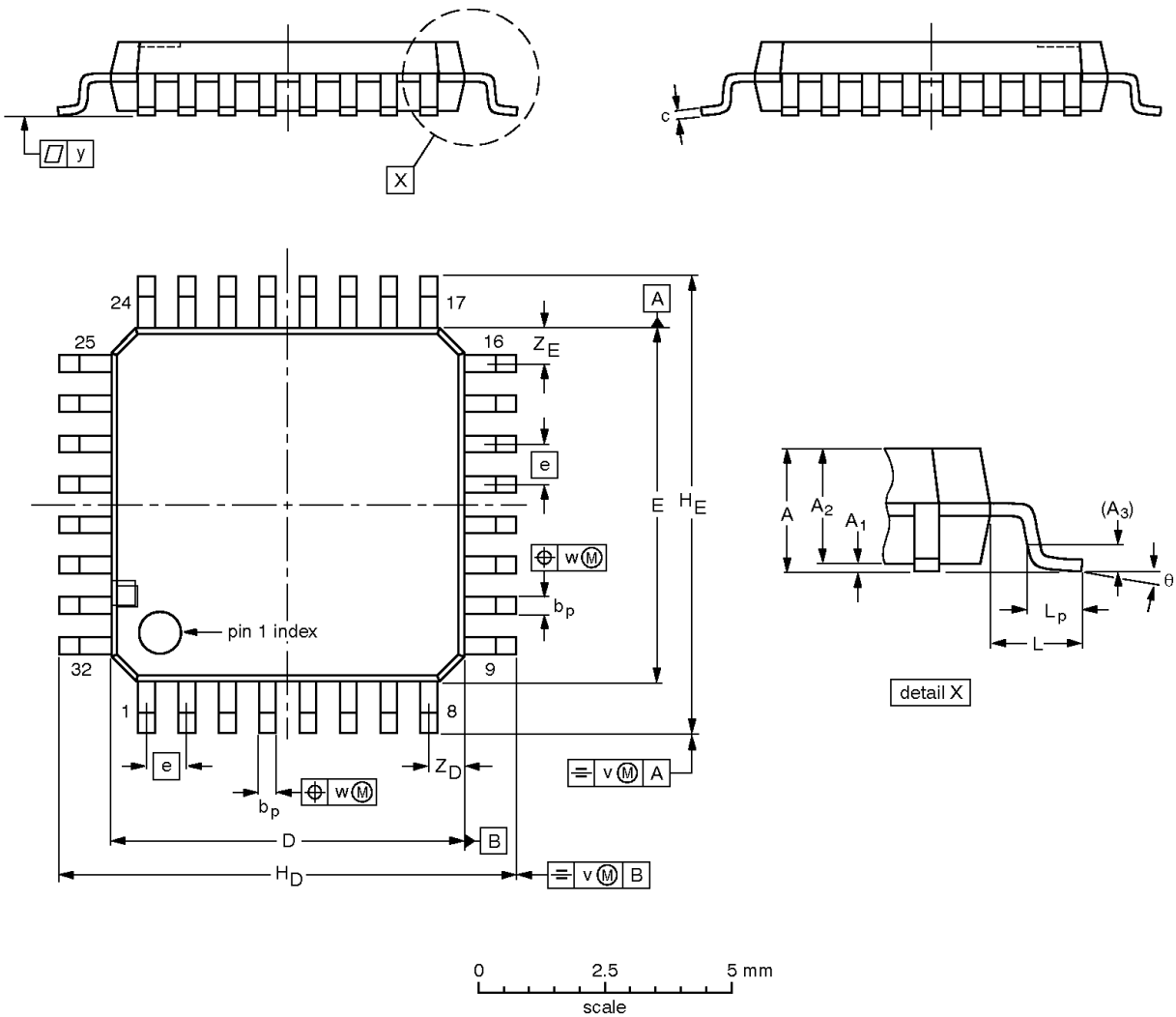


Figure 4. Optimized dual line termination

SPICE level output buffer models are available for engineers who want to simulate their specific interconnect schemes. In addition, IV characteristics are in the process of being generated to support the other board-level simulators in general use.

LQFP32: plastic low profile quad flat package; 32 leads; body 7 x 7 x 1.4 mm **SOT358-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_D	H_E	L	L_p	v	w	y	$Z_D^{(1)}$	$Z_E^{(1)}$	θ
mm	1.6	0.20 0.05	1.45 1.35	0.25	0.4 0.3	0.18 0.12	7.1 6.9	7.1 6.9	0.8	9.15 8.85	9.15 8.85	1	0.75 0.45	0.2	0.25	0.1	0.9 0.5	0.9 0.5	7^o 0^o

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT358 -1	136E03	MS-026				~~00-01-19~~ 03-02-25

REVISION HISTORY

Rev	Date	Description
_4	20030731	**Product data (9397 750 11762); ECN 853-2222 30050 dated 18 June 2003. Supersedes data of 02 May 2003 (9397 750 11465).** Modifications: • Minor changes or corrections to existing product specifications.
_3	20030502	Product data (9397 750 11465); ECN 853-2222 29827 dated 02 May 2003. Supersedes data of 2001 Feb 08 (9397 750 08062).
_2	20010208	Product data (9397 750 08062); ECN 853-2222 25600 Dated 2001 Feb 08. Supersedes data of 2000 Oct 25.

20-125 MHz PECL input / 9 CMOS output 3.3 V PLL clock driver

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Level	Data sheet status[1]	Product status[2] [3]	Definitions
I	Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
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